Electronic Version
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Claims

[c1] WHAT IS CLAIMED IS:

1. A motor control circuit for supplying a driving voltage to a motor, the motor having a first terminal and a second terminal, the driving voltage being applied between the first and the second terminals, the motor control circuit comprising:

an H-bridge circuit having a first linear unit, a second linear unit, a first switching unit, and a second switching unit, the first linear unit and the first switching unit being together coupled to the first terminal and the second linear unit and the second switching unit being together coupled to the second terminal;

a voltage detection circuit for generating at least one voltage detection signal representative of the driving voltage of the motor;

an error amplifier for generating at least one error signal representative of a difference between the at least one voltage detection signal and a command voltage signal, the at least one error signal being electrically separate from the first and the second switching units;

a feedback circuit coupled to the error amplifier for receiving the at least one error signal so as to apply the at

least one error signal selectively to the first or the second linear unit; and

a state control circuit for synchronously controlling the first and the second switching units and the feedback circuit such that during a first operational period the first switching unit is operated in a nonconductive mode, the second switching unit is operated in a conductive mode, the feedback circuit allows one of the at least one error signal to be applied to the first linear unit for operating the first linear unit in a linear mode, and the feedback circuit prevents the at least one error signal from being applied to the second linear unit, thereby controlling the driving voltage to become substantially proportional to the command voltage signal.

[c2] 2. The motor control circuit according to claim 1, wherein:

during the first operational period, the driving voltage causes a current to flow through the motor in a direction from the first terminal toward the second terminal.

[c3] 3. The motor control circuit according to claim 1, wherein:

the first and the second linear units are further coupled to a supply voltage source, and

the first and the second switching units are further coupled to a ground potential.

[c4] 4. The motor control circuit according to claim 1, wherein:
the voltage detection circuit includes:
a first voltage divider connected between the first terminal and a ground potential for outputting a first terminal division voltage signal as one of the at least one voltage detection signal, and
a second voltage divider connected between the second terminal and the ground potential for outputting a second terminal division voltage as another of the at least one voltage detection signal.

[c5] 5. The motor control circuit according to claim 4, wherein:
the error amplifier includes:
a first NMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being controlled by the first terminal division voltage signal and the source electrode being coupled to a constant current source;
a second NMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being controlled by the second terminal division voltage signal and the source electrode being coupled to the constant current source;
a third NMOS transistor having a gate electrode, a drain

electrode, and a source electrode, the gate electrode being controlled by the command voltage signal and the source electrode being coupled to the constant current source;

a first current mirror having an original current branch and a mirror current branch, the original current branch being coupled to the drain electrode of the first NMOS transistor and the drain electrode of the second NMOS transistor;

a second current mirror having an original current branch and a mirror current branch, the original current branch being coupled to the drain electrode of the third NMOS transistor;

a third current mirror having an original current branch and a mirror current branch, the original current branch being coupled to the mirror current branch of the first current mirror; and

a first output terminal coupled to the mirror current branch of the second current mirror and the mirror current branch of the third current mirror for supplying the one of the at least one error signal.

[c6] 6. The motor control circuit according to claim 5, wherein:

the original current branch of the first current mirror is implemented by a first PMOS transistor having a gate

electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the drain electrode, the drain electrode being coupled to the drain electrode of the first NMOS transistor and the drain electrode of the second NMOS transistor, and the source electrode being coupled to a constant voltage source;

the original current branch of the second current mirror is implemented by a second PMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the drain electrode, the drain electrode being coupled to the drain electrode of the third NMOS transistor, and the source electrode being coupled to the constant voltage source;

the mirror current branch of the first current mirror is implemented by a third PMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the gate electrode of the original current branch of the first current mirror, the drain electrode being coupled to the original current branch of the third current mirror, and the source electrode being coupled to the constant voltage source; and

the mirror current branch of the second current mirror is implemented by a fourth PMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the gate electrode of the original current branch of the second current mirror, the

drain electrode being coupled to the first output terminal of the error amplifier, and the source electrode being coupled to the constant voltage source.

[c7] 7.The motor control circuit according to claim 5, wherein:
the original current branch of the third current mirror is implemented by a fourth NMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the drain electrode, the drain electrode being coupled to the mirror current branch of the first current mirror, and the source electrode being coupled to a ground potential, and
the mirror current branch of the third current mirror is implemented by a fifth NMOS transistor having a gate electrode, a drain electrode, and a source electrode, the gate electrode being coupled to the gate electrode of the fourth NMOS transistor, the drain electrode being coupled to the mirror current branch of the second current mirror, and the source electrode being coupled to the ground potential.

[c8] 8.The motor control circuit according to claim 1, wherein:
the feedback circuit includes:
a first switching means coupled to the first linear unit and controlled by the state control circuit for allowing

the one of the at least one error signal to be applied to the first linear unit during the first operational period, and

a second switching means coupled to the second linear unit and controlled by the state control circuit for preventing the at least one error signal from being applied to the second linear unit during the first operational period.

[c9] 9.The motor control circuit according to claim 1, wherein:

the feedback circuit includes:

a first capacitor coupled to the first linear unit for causing the one of the at least one error signal to be relatively gradually applied to the first linear unit during the first operational period.

[c10] 10.The motor control circuit according to claim 1, wherein:

the state control circuit synchronously outputs a first, a second, a third, and a fourth state control signals, for controlling the feedback circuit and the first and the second switching units of the H-bridge circuit, respectively, each of the first to the fourth state control signals being a digital logic signal having a logic high level and a logic low level, and

during the first operational period, the first and the third

state control signals are at the logic low level and the second and the fourth state control signals are at the logic high level.

[c11] 11.The motor control circuit according to claim 1, wherein:
the state control circuit further synchronously controls the first and the second switching units and the feedback circuit such that during a second operational period the first switching unit is operated in the conductive mode, the second switching unit is operated in the nonconductive mode, the feedback circuit prevents the at least one error signal from being applied to the first linear unit, and the feedback circuit allows another of the at least one error signal to be applied to the second linear unit for operating the second linear unit in the linear mode, thereby controlling the driving voltage to become substantially proportional to the command voltage signal.

[c12] 12.The motor control circuit according to claim 11, wherein:
during the second operational period, the driving voltage causes a current to flow through the motor in a direction from the second terminal toward the first terminal.

[c13] 13.The motor control circuit according to claim 11, wherein:

the second current mirror further has a parallel mirror current branch coupled in parallel with the mirror current branch of the second current mirror;
the third current mirror further has a parallel mirror current branch coupled in parallel with the mirror current branch of the third current mirror; and
the error amplifier further includes a second output terminal coupled to the parallel mirror current branch of the second current mirror and the parallel mirror current branch of the third current mirror, for supplying the another of the at least one error signal.

[c14] 14.The motor control circuit according to claim 11, wherein:
the feedback circuit includes:
a first switching means coupled to the first linear unit and controlled by the state control circuit, for allowing the one of the at least one error signal to be applied to the first linear unit during the first operational period and for preventing the at least one error signal from being applied to the first linear unit during the second operational period, and
a second switching means coupled to the second linear unit and controlled by the state control circuit, for preventing the at least one error signal from being applied to the second linear unit during the first operational pe-

riod and for allowing the another of the at least one error signal to be applied to the second linear unit during the second operational period.

[c15] 15.The motor control circuit according to claim 11, wherein:
the feedback circuit includes:
a first capacitor coupled to the first linear unit for causing the one of the at least one error signal to be relatively gradually applied to the first linear unit during the first operational period, and
a second capacitor coupled to the second linear unit for causing the another of the at least one error signal to be relatively gradually applied to the second linear unit during the second operational period.

[c16] 16. The motor control circuit according to claim 11, wherein:
the state control circuit synchronously outputs a first, a second, a third, and a fourth state control signals, for controlling the feedback circuit and the first and the second switching units of the H-bridge circuit, respectively, each of the first to fourth state control signals being a digital logic signal having a logic high level and a logic low level, such that:
during the first operational period, the first and the third state control signals are at the logic low level and the

second and the fourth state control signals are at the logic high level, and
during the second operational period, the first and the third state control signals are at the logic high level and the second and the fourth state control signals are at the logic low level.

[c17] 17. The motor control circuit according to claim 1, further comprising:
a brake circuit controlled by the state control circuit such that during a third operational period the brake circuit transforms the at least one error signal to become at least one brake signal for being simultaneously applied to the first and the second linear units through the feedback circuit to operate the first and the second linear units in the conductive mode, and
during the third operational period, the state control circuit operates the first and the second switching units in the nonconductive mode.

[c18] 18.The motor control circuit according to claim 17, wherein:
the error amplifier has at least one inverting input terminal for receiving the at least one voltage detection signal, respectively, and a non-inverting input terminal for receiving the command voltage signal, and
during the third operational period, the brake circuit

connects the at least one inverting input terminal in short circuit to the ground potential such that the at least one error signal is transformed to become the at least one brake signal.

[c19] 19.The motor control circuit according to claim 18, wherein:
the error amplifier further has at least one output terminal for outputting the at least one error signal, respectively, and
during the third operational period, the brake circuit causes the at least one output terminal to rapidly transform the at least one error signal to become the at least one brake signal.

[c20] 20. The motor control circuit according to claim 17, wherein:
the state control circuit synchronously outputs a first, a second, a third, a fourth state control signals, and a brake control signal, the first to the fourth state control signals being used to control the feedback circuit and the first and the second switching units of the H-bridge circuit, respectively, and the brake control signal being applied to the brake circuit such that the brake circuit transforms the at least one error signal to become the at least one brake signal, each of the first to the fourth state control signals and the brake control signal being a

digital logic signal having a logic high level and a logic low level, such that:

during the first operational period, the first and the third state control signals are at the logic low level, the second and the fourth state control signals are at the logic high level, and the brake control signal is at the logic low level, and

during the third operational period, the first to the fourth state control signals are at the logic low level and the brake control signal is at the logic high level.